UCIe™ (Universal Chiplet Interconnect Express™)

Accelerating the future of semiconductor innovations in an open source environment

Presented by
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UCIe™
Universal Chiplet Interconnect Express

Agenda

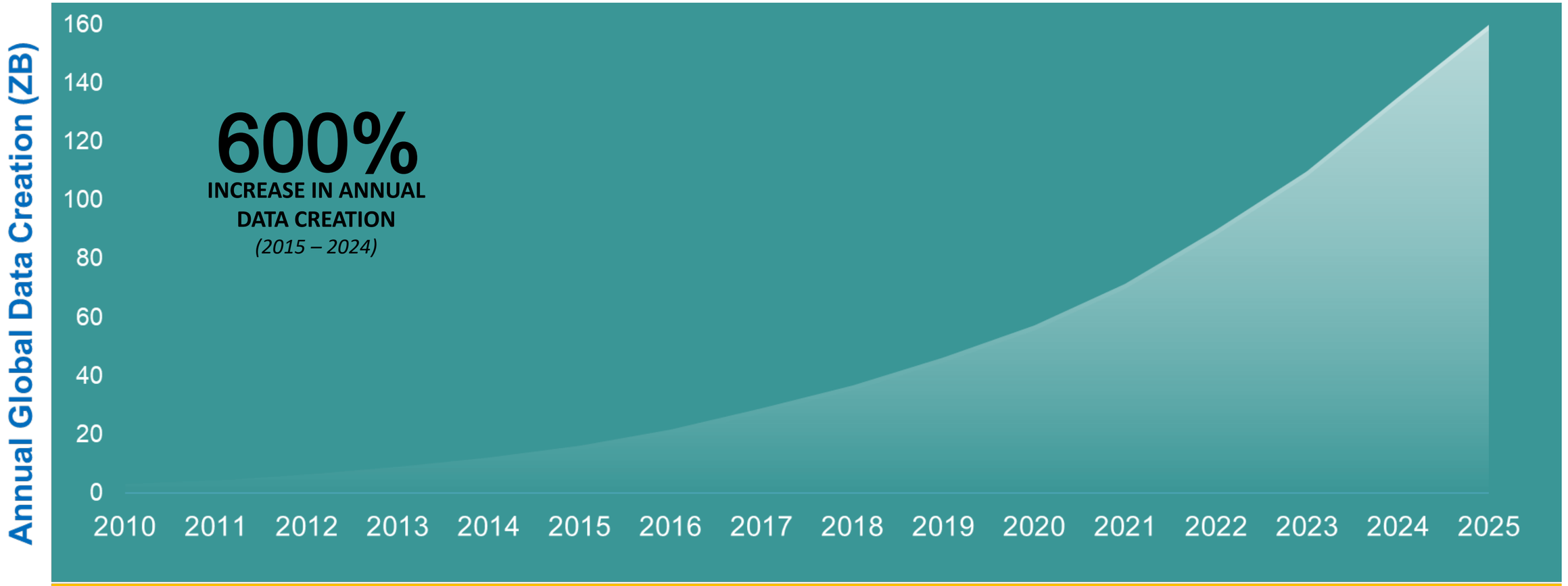
- Interconnects in Compute Landscape
- UCIe (Universal Chiplet Interconnect Express): An Open Standard for Chiplets
- Future Directions and Conclusions

Industry landscape

Industry mega-trends are driving demand for faster data processing and more memory capacity / bandwidth

Explosion of data enabling data-centric revolution

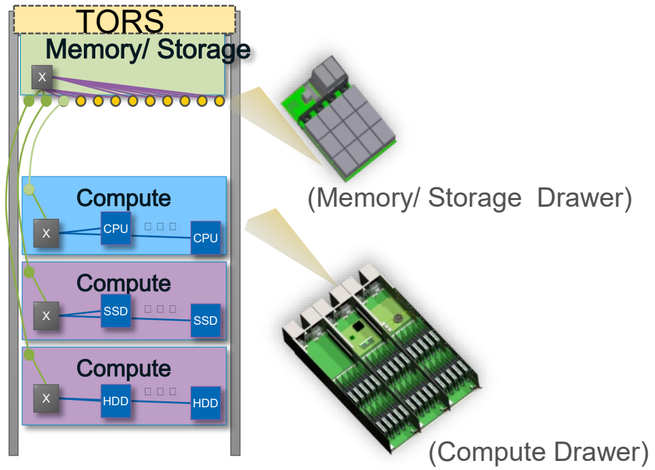
Source: IDC Data Age 2025



Drivers: Cloud, 5G, sensors, automotive, IoT, etc.. Large data sets with aggressive time to insight goals!
Scaling challenges: Latency, Bandwidth, Capacity all important!
Move faster, Store more, Process everything seamlessly, efficiently, and securely

Cloud computing landscape today

(Rack of Servers)

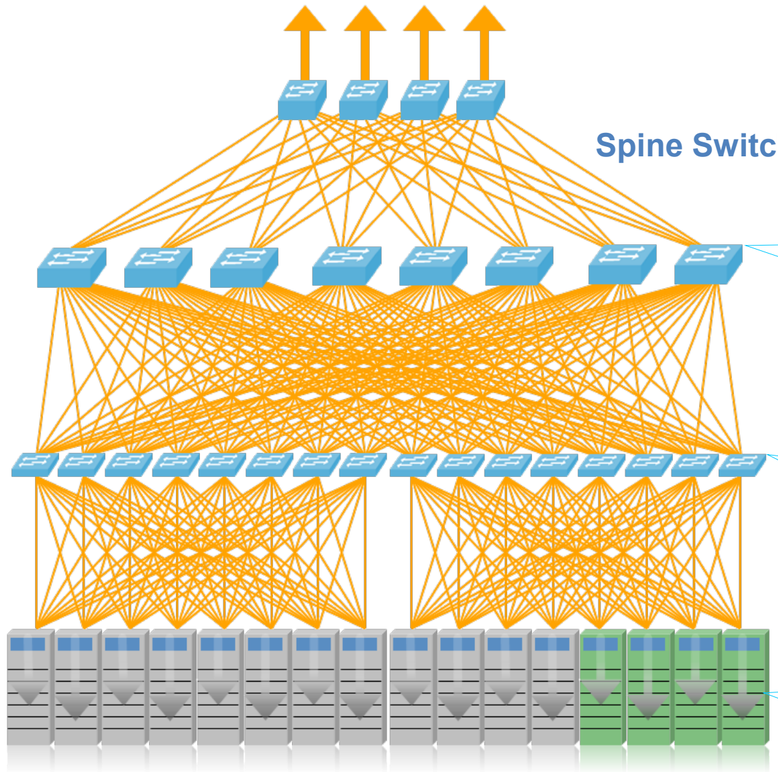


(Memory/ Storage Drawer)

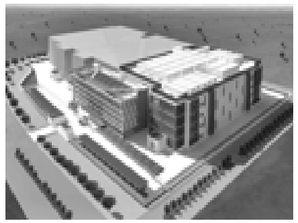
(Compute Drawer)

Ld/ St I/O inside drawer and Rack

Core/ Edge Network & Inter-DC Network



Hyperscale Data Center and Edge



Silicon Photonics

High-bandwidth connectivity at 100G and beyond

Programmable Switching

P4-programmable scale-out fabric with uncompromising performance

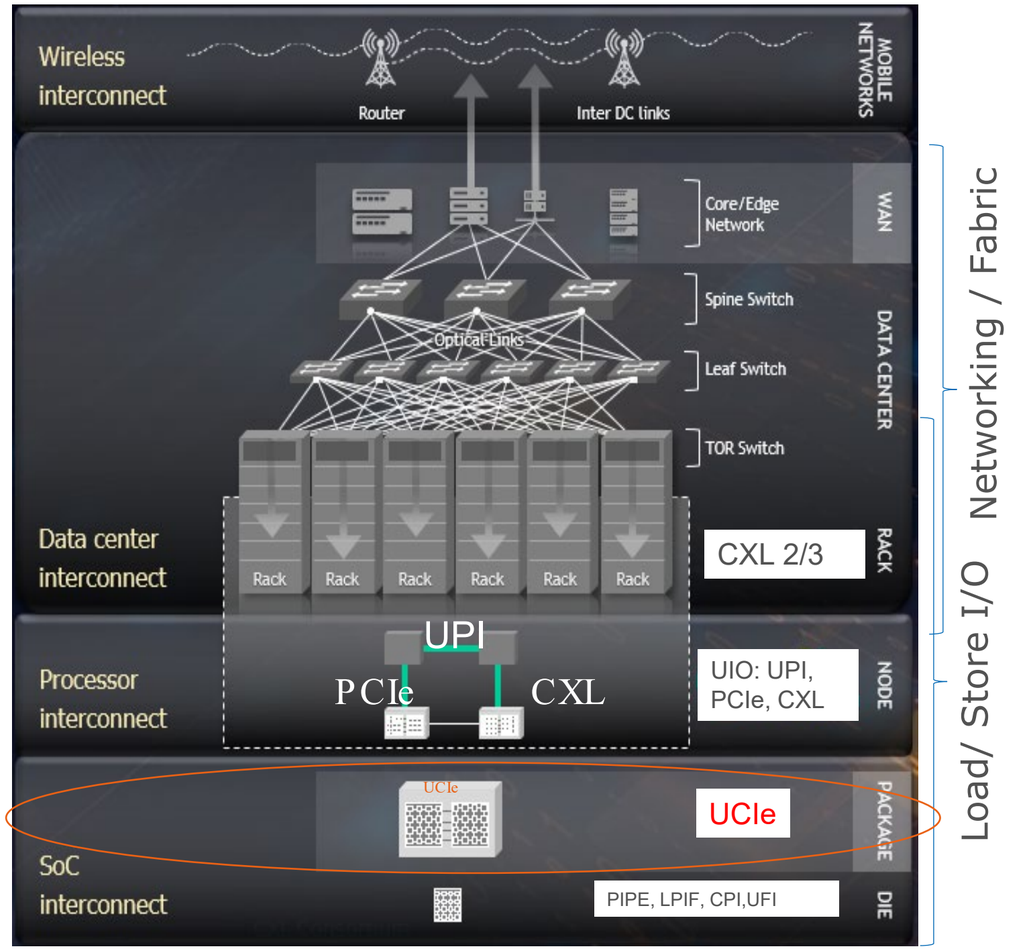
Rack of Servers

Programmable infrastructure acceleration for demanding data movement with Smart NIC

Data Center as a Computer –Interconnects are key to driving warehouse scale efficiency!

Taxonomy, characteristics, and trends of interconnects

	Category	Type and Scale	Data Rate/ Characteristics	PHY Latency (Tx + Rx)
Off-Package	Latency Tolerant (Narrow, very high speed)	Networking / Fabric for Data Center Scale	56/ 112 GT/s-> 224 GT/s (PAM4) 4-8 Lanes, cables/ backplane	20+ ns (+ >100 FEC)
Off-Package	Latency Sensitive (Wide, high speed)	Load-Store I/O Arch. Ordering (PCIe/ CXL / SMP cache coherency – PCIe PHY) Node (-> Rack)	32 GT/s (NRZ) -> PCIe Gen6 64 GT/s (PAM4) Hundreds of Lanes Power, Cost, Si-Area, Backwards Compatible, Latency, On-board -> cables/ backplanes	<10ns (Tx+ Rx: PHY-PIPE) 0-1ns FEC overhead
On-Package	Latency Sensitive (super-wide, high speed)	Load-Store and proprietary	4 G – 32G (single-ended, NRZ) 2D, 2.5D (-> 3D) Thousands of Lanes Ultra low power, ultra low latency High b/w density	<2ns (PHY – Transaction Layer)



Load-Store I/O: From Package/ Node to Rack / Pod

Load-Store interconnects: PCIe and CXL

With PCIe®: (900+ member companies)

- Memory Connected to CPU – Cacheable
- Memory Connected to PCIe device is Uncacheable
- Different Ordering rules across I/O vs coherency domains
- Ubiquitous I/O for compute continuum

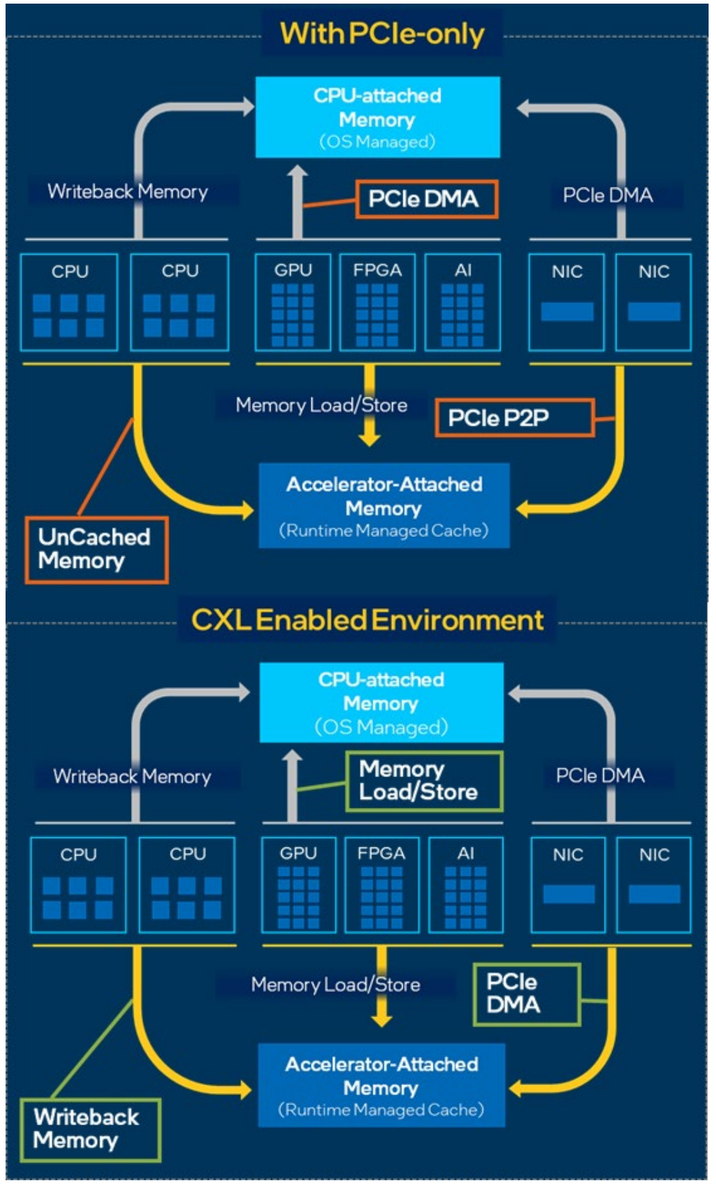
With CXL™: (~200 member companies)

- Caching and memory protocols on top of PCIe
- Device can cache memory
- Memory attached to device is cacheable
- Leverages PCIe infrastructure

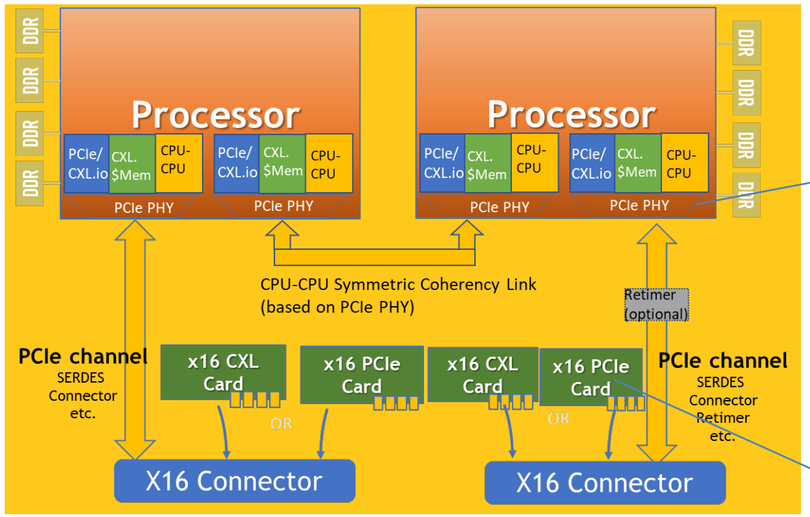
PCIe and CXL very successful industry standards:

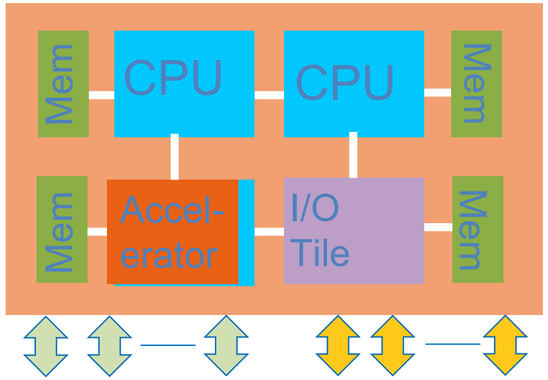
- Multi-generational, backward compatible, IP/ tools
- Compliance program with plug-and-play

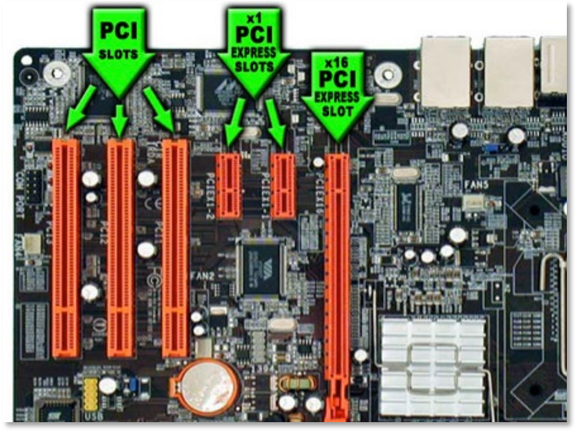
On-Package Interconnects should leverage PCIe/CXL infrastructure for standardization and Load-Store Usages. Need to seamlessly move functionality from node to package to die level.



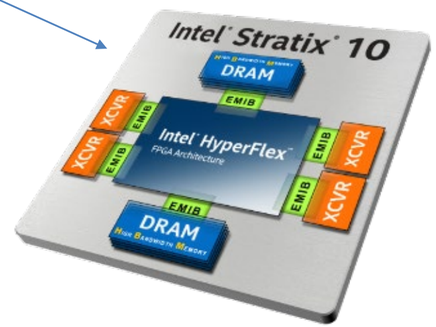
Seamless integration from Node to Package to On-Die for reuse and better user experience



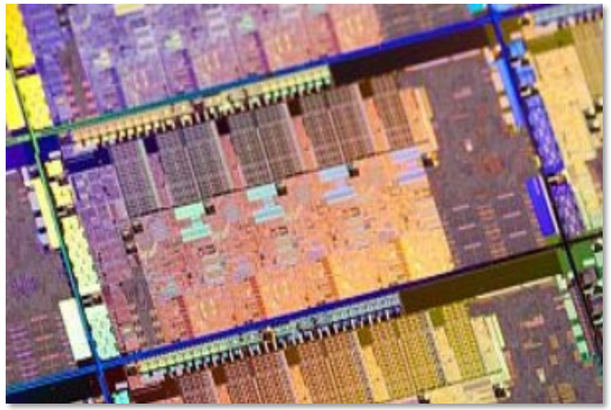




(Node/Board Level)



(Package Level Integration)



(On-die Integration)

Same Software, IP, and Subsystem to build scalable solutions offers economies of scale, Time to Market Advantage, and a seamless user experience.

Agenda

- Interconnects in Compute Landscape
- **UCIe (Universal Chiplet Interconnect Express): An Open Standard for Chiplets**
- Future Directions and Conclusions

Moore Predicted "Day of Reckoning"

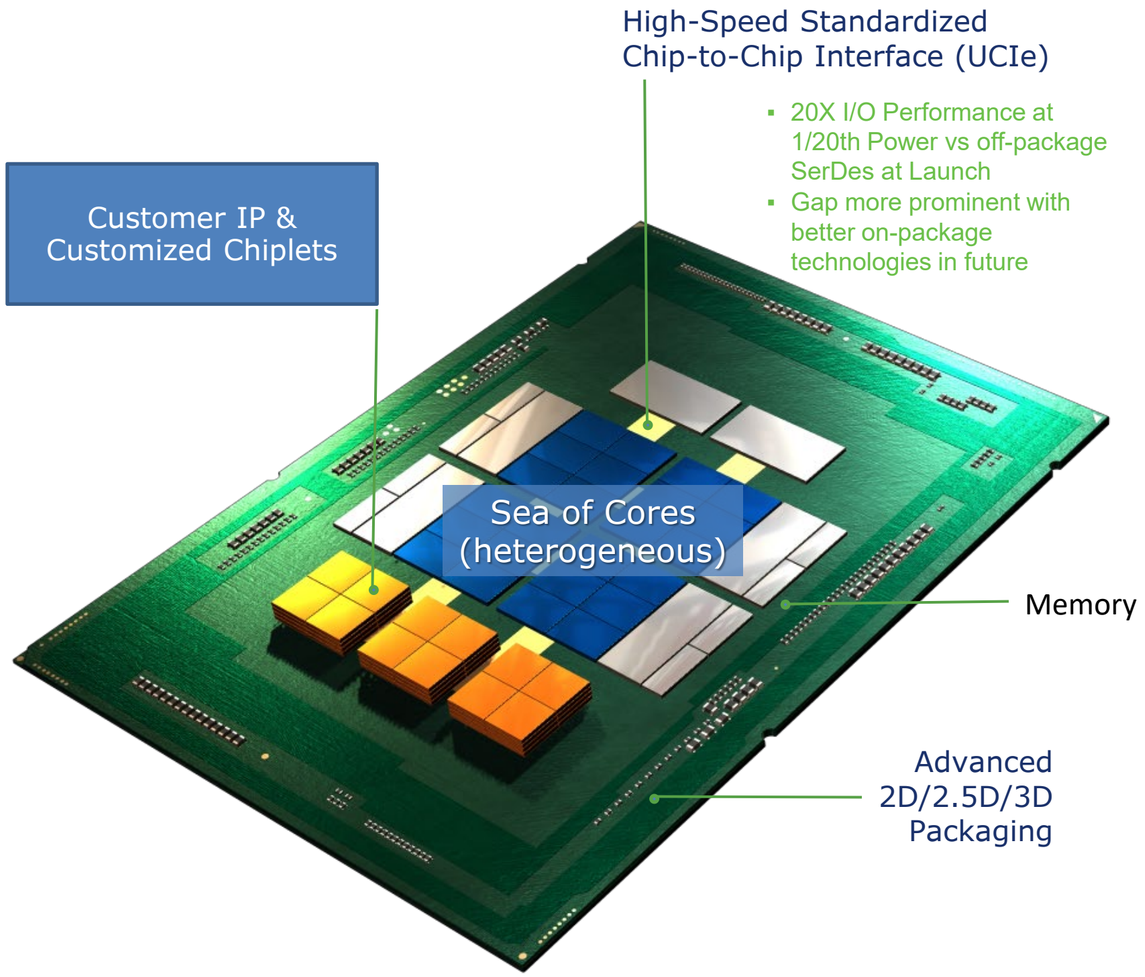
*"It may prove to be more economical to build large systems out of smaller functions, which are separately packaged and interconnected."**

- Gordon E. Moore

*"Cramming more components onto integrated circuits," Electronics, Volume 38, Number 8, April 19, 1965

Motivation

OPEN CHIPLET: PLATFORM ON A PACKAGE

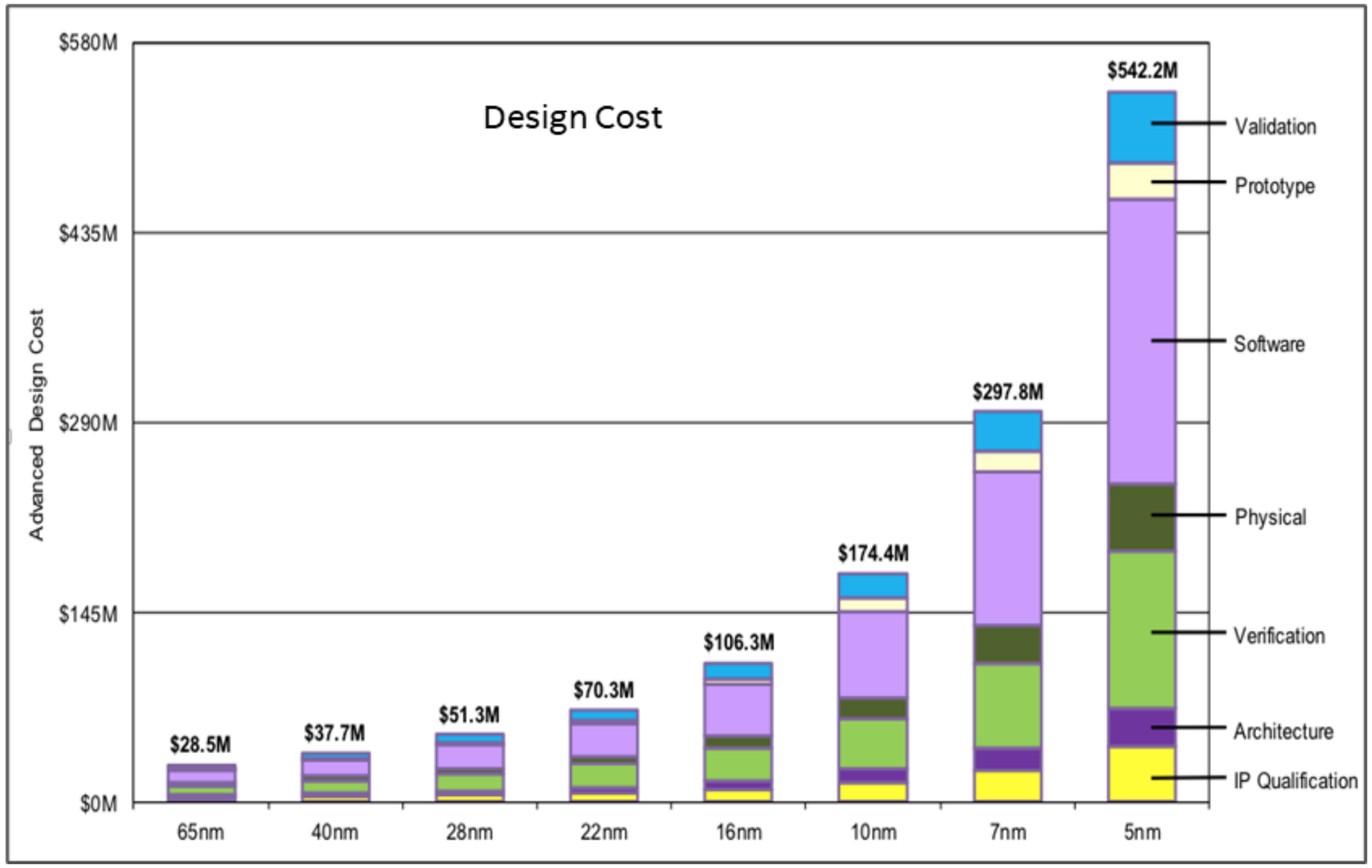


Heterogeneous Integration Fueled by an Open Chiplet Ecosystem
(Mix-and-match chiplets from different process nodes / fabs / companies / assembly)

Align Industry around an open platform to enable chiplet based solutions

- Enables construction of SoCs that exceed maximum reticle size
  - Package becomes new System-on-a-Chip (SoC) with same dies (Scale Up)
- Reduces time-to-solution (e.g., enables die reuse)
- Lowers portfolio cost (product & project)
  - Enables optimal process technologies
  - Smaller (better yield)
  - Reduces IP porting costs
  - Lowers product SKU cost
- Enables a customizable, standard-based product for specific use cases (bespoke solutions)
- Scales innovation (manufacturing and process locked IPs)

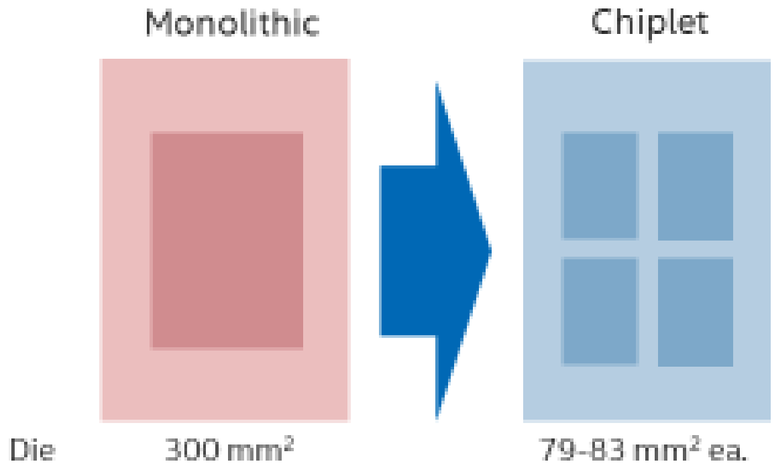
UCIe ameliorates the increased design costs



Source: IBS (as cited in IEEE Heterogeneous Integration Roadmap)

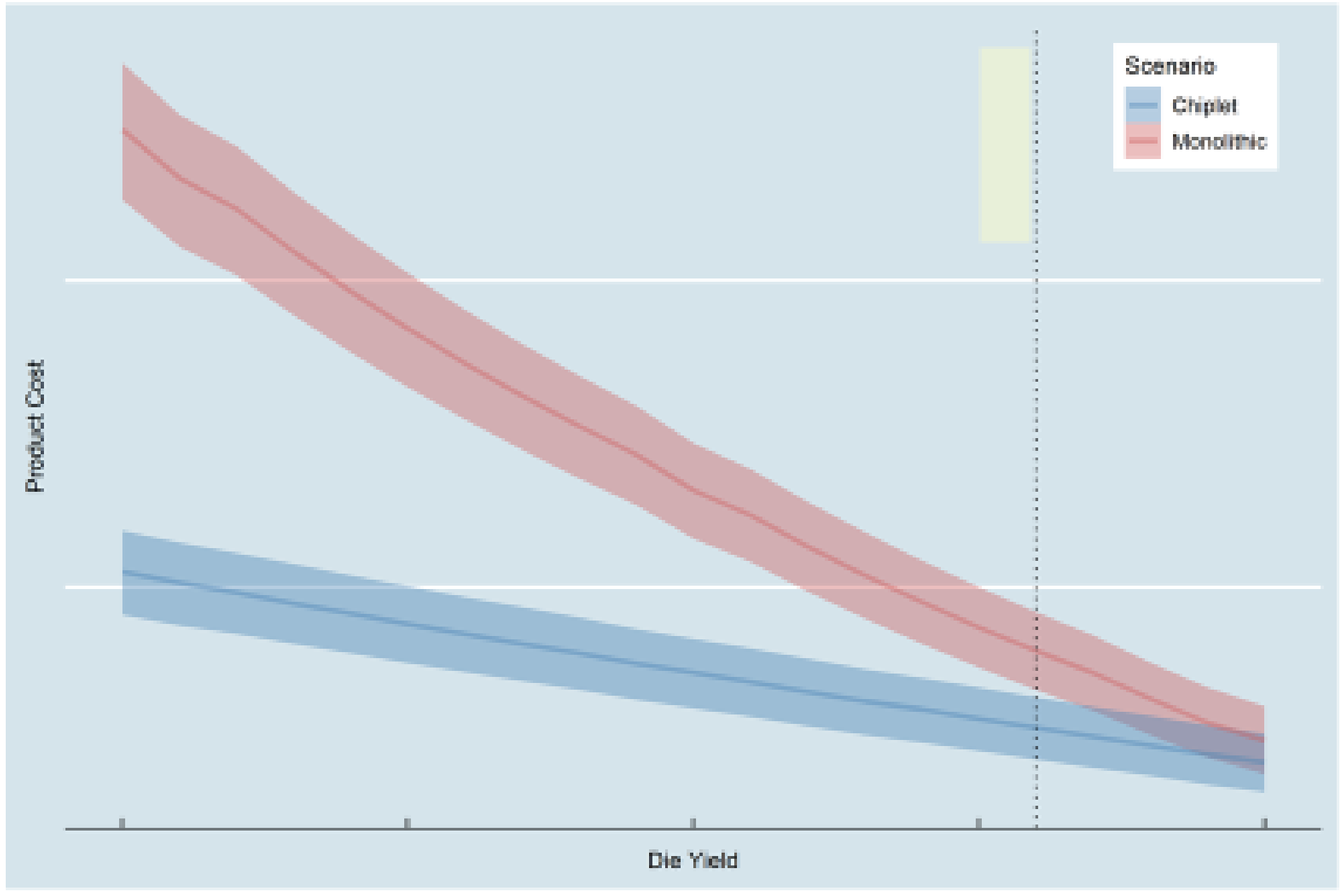
UCIe enables mix-and-match chiplets: reuse old chiplets whose functionality has not changed

Motivation: Cost & Manufacturing Optimization



Input Variables:

- Die Area
- # of Chiplets
- Wafer Cost
- Defect Density
- Package/Assembly/Test
- Known Good Die
- Die Area Tax & Overhead



*Probabilistic trend by 1std dev

: https://ieeexplore.ieee.org/document/9758914

Key Metrics and Adoption Criteria

UCIe - Architected and specified from the ground-up to deliver the best KPIs while meeting wide adoption criteria

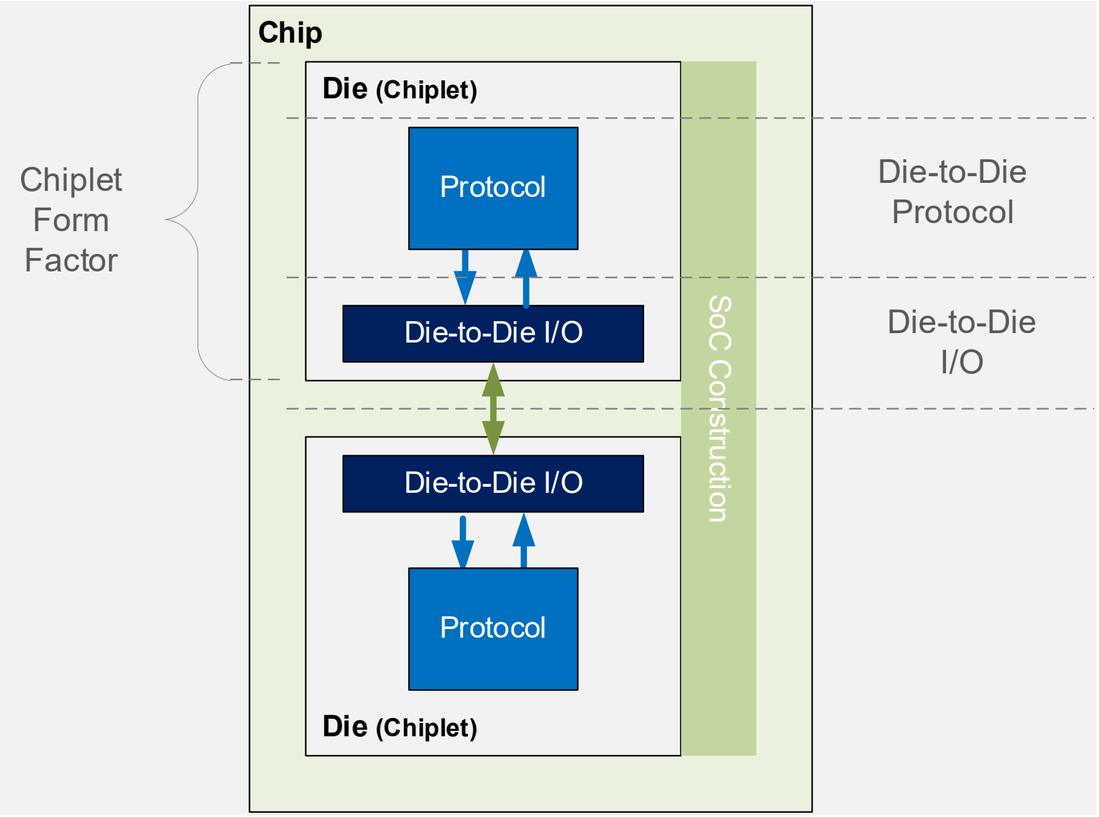
Key Performance Indicators

- Bandwidth density (linear & area)
  - Data Rate & Bump Pitch
- Energy Efficiency (pJ/b)
  - Scalable energy consumption
  - Low idle power (entry/exit time)
- Latency (end-to-end: Tx+Rx)
- Channel Reach
  - Technology, frequency, & BER
- Reliability & Availability
- Cost
  - Standard vs advanced packaging

Factors Affecting Wide Adoption

- Interoperability
  - Full-stack, plug-and-play with existing s/w is+
  - Different usages/segments
  - Technology
    - Across process nodes & packaging options
    - Power delivery & cooling
    - Repair strategy (failure/yield improvement)
    - Debug – controllability & observability
  - Broad industry support / Open ecosystem
    - Learnings from other standards efforts

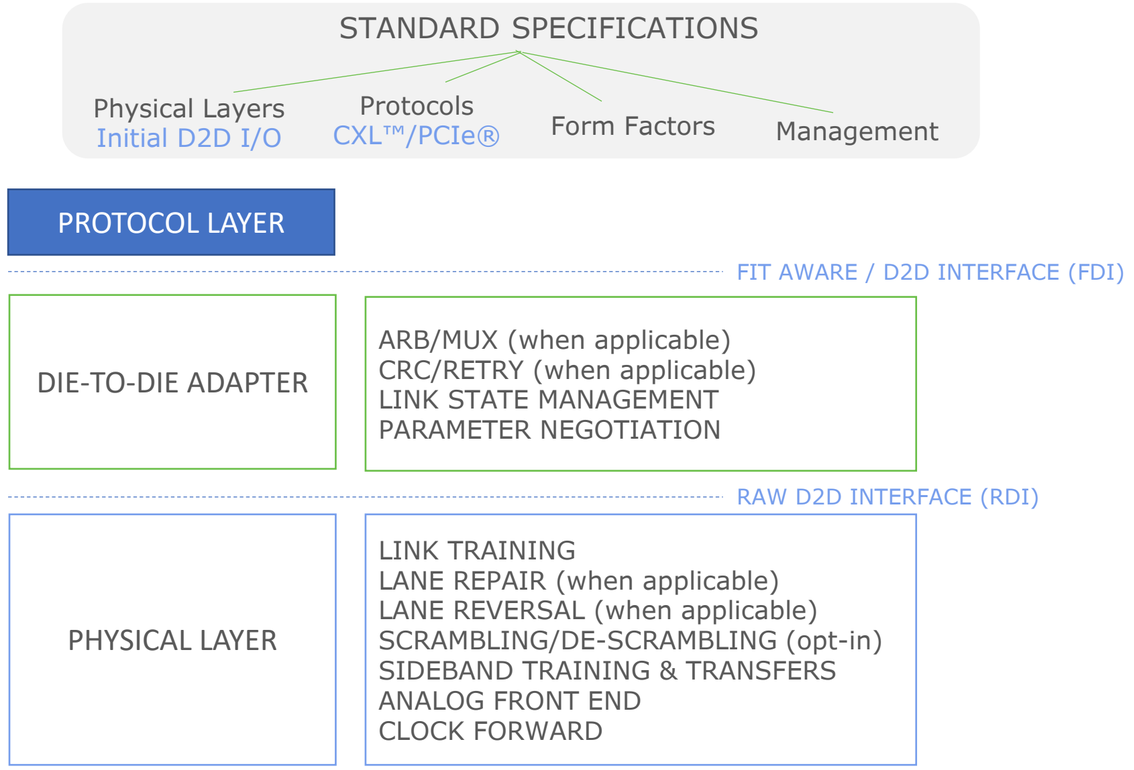
Components of chiplet interoperability



- **Chiplet Form Factor**
  - Die size
  - Bump location
  - Power delivery
  - Thermal characteristics
- **SoC Construction (Application Layer)**
  - SoC Reset
  - Initialization (e.g., fuses)
  - Register access
  - Security
- **Die-to-Die Protocols (Data Link to Transaction Layer)**
  - Link Layer, transaction Layer, etc.: PCIe/ CXL/ Raw/….
  - Internal Interface standardization for plug and play IPs
- **Die-to-Die I/O (Physical Layer)**
  - Bump arrangement and characteristics
  - Electrical & thermal characteristics
  - Substrate or interposer characteristics
  - Length budget, pJ/bit, bit error rate, …
  - Reset, clocking, initialization, and data transfer
  - Test and repair
  - Technology transition -> multiple bump arrangement/ frequency

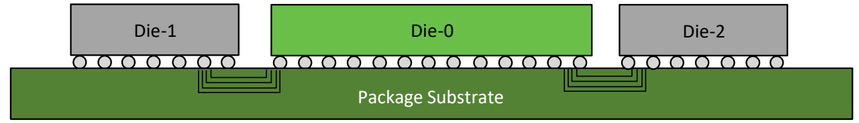
Jumpstarting UCIe

- **Focus of UCIe 1.0 Specification**
  - **Physical Layer:** Die-to-Die I/O with industry-leading KPIs
  - **Protocol:** CXL™/PCIe® for near term volume attach
    - SoC construction issues are addressed since CXL/PCIe is a board-to-board interface
    - CXL/PCIe addresses common use cases
      - I/O attach with PCIe/CXL.io
      - Memory use cases: CXL.mem
      - Accelerator use cases: CXL.cache
  - **Well defined specification**: ensure interoperability and future evolution

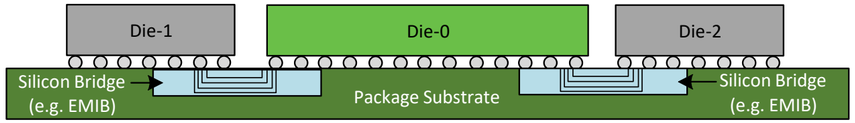


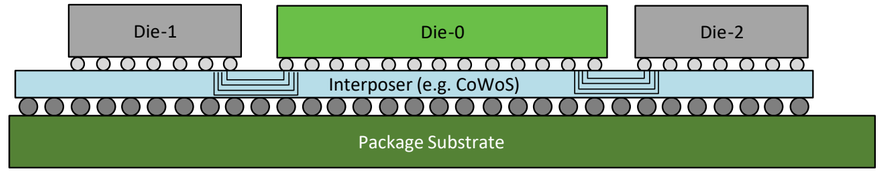
UCIe 1.0: Supports standard and advanced packages

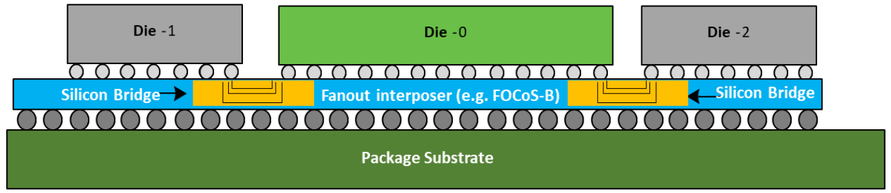
- **Standard Package: 2D – cost effective, longer distance**
- **Advanced Package: 2.5D – power-efficient, high bandwidth density**
- **Dies can be manufactured anywhere and assembled anywhere – can mix 2D and 2.5D in same package – Flexibility for SoC designer**



(Standard Package)







(Multiple Advanced Package Choices)

One UCIe 1.0 Spec covers both type of packaging options.

Layering approach of UCIe

Distinct Layering approach => ease of implementation and backward compatible evolution

Protocol Layer:

- PCIe 6.0, CXL 2.0, and CXL 3.0 protocols: plug and play with existing ecosystem including CSR compatibility
- Streaming protocol: any protocol including raw bits
- Connects to D2D Adapter through a well-defined interface

Die to Die Adapter:

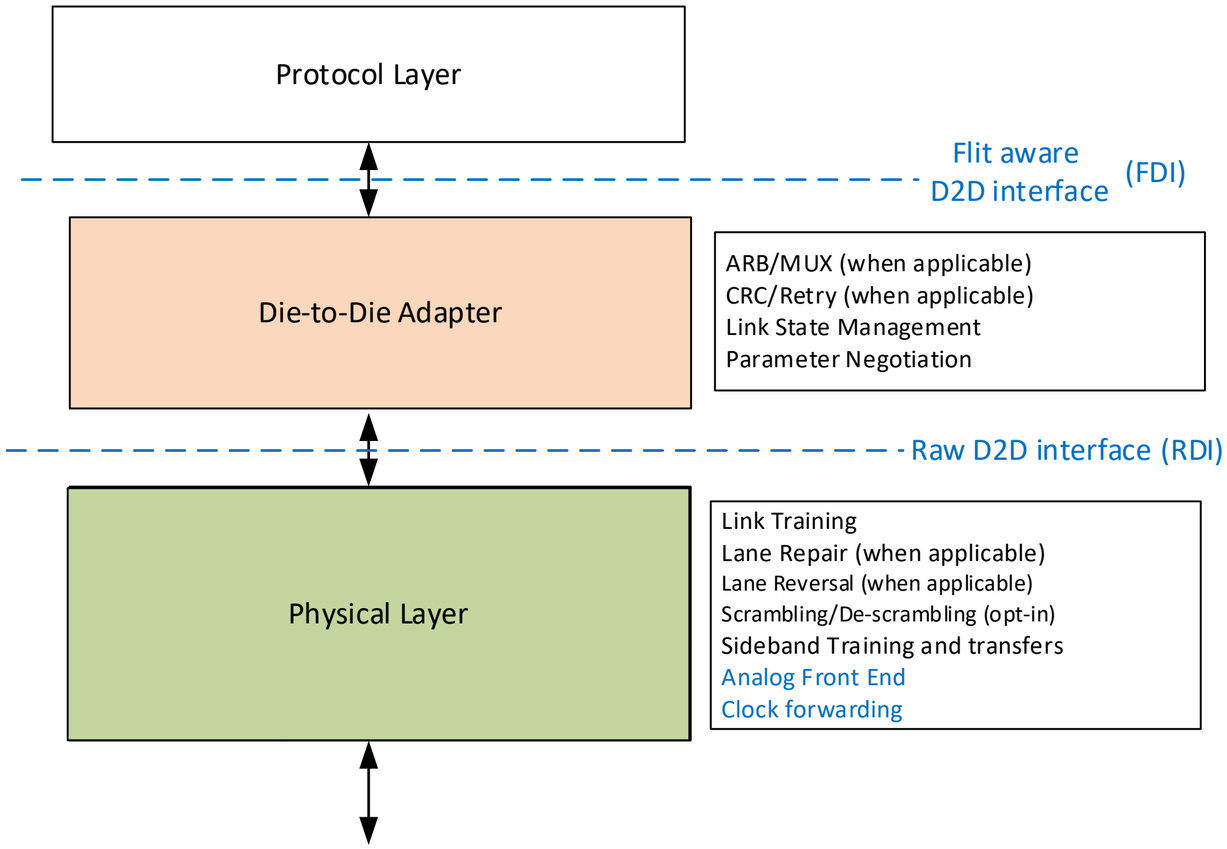
- Initial Protocol / Parameter negotiation
- Multiplexing multiple protocols when needed
- Reliable data transfer (CRC/ Retry/ Flit)
- Link state / Power state management

PHY Layer: Physical transmit/receive, init, etc.

- PHY Logical
- Electrical/ AFE
- Sideband/ Global

Config Register

- Uses PCIe infrastructure for plug and play
- Distinct set of registers for the PHY and D2D adapters – but default mapping to PCIe so that UCIe-unaware software can still run



UCIe PHY

Electrical AFE for main-band and side band

- FIFO for clock drift, SERDES, Clocking, Tx/ Rx circuits

Logical PHY

- Link training, Lane repair/ degrade, Lane reversal, Scrambling, Sideband training

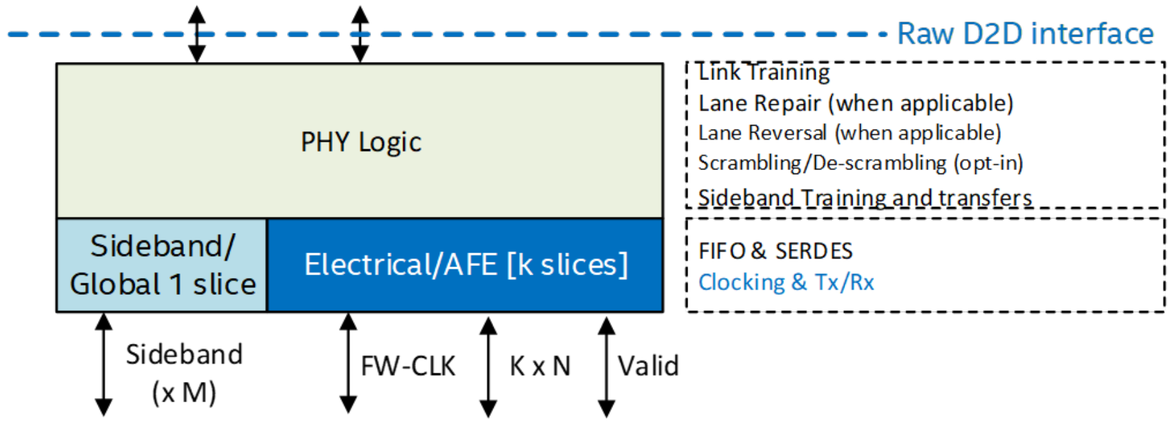
Main data path: One Data Slice per direction

- 16 Lanes (64 lanes) for standard (advanced) packaging
- 1 Lane of valid
- 1 differential pair of forwarded clock
- 1 Lane for background calibration

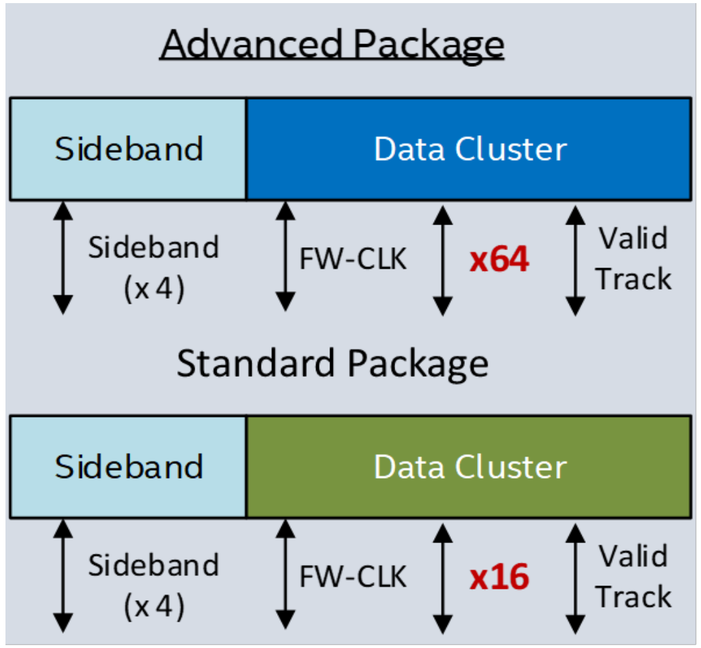
Sideband/Global slice per direction :

- 2 Lanes (1 Data and 1 Clock)
- Can be shared across multiple Data slices (up to 4)
- Fixed speed 800MHz from aux clock (always on)
- Aux power domain
- Used for Link Training, CSR accesses, etc.

Standard RDI interface to D2D Adapter



UCIe: Configuration and RAS



Die - 1		Die - 2			
x16	<-->	x16	CL-0 x16	<-->	CL-0 x16
x32	<-->	x32	CL-0 x16	<-->	CL-0 x16
			CL-1 x16	<-->	CL-1 x16
x64	<-->	x64	CL-0 x16	<-->	CL-0 x16
			CL-1 x16	<-->	CL-1 x16
			CL-2 x16	<-->	CL-2 x16
			CL-3 x16	<-->	CL-3 x16

(1, 2, or 4 Clusters can be combined in one UCIe Link)

RAS Feature	Standard	Advanced
Lane repair	No	Yes
Lane reversal	Yes	Yes
Width degrade	Yes	No

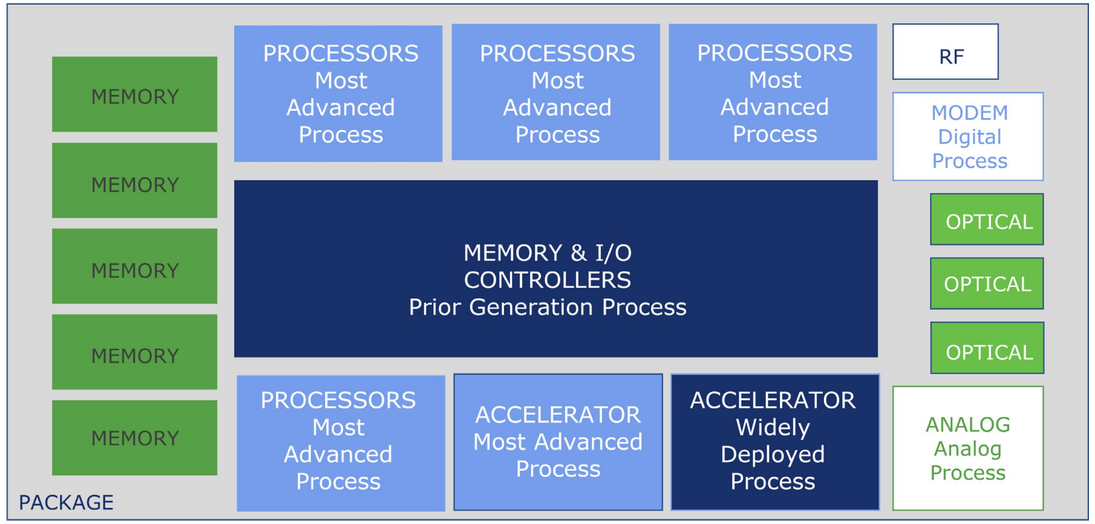
UCIe usage model: SoC at package level

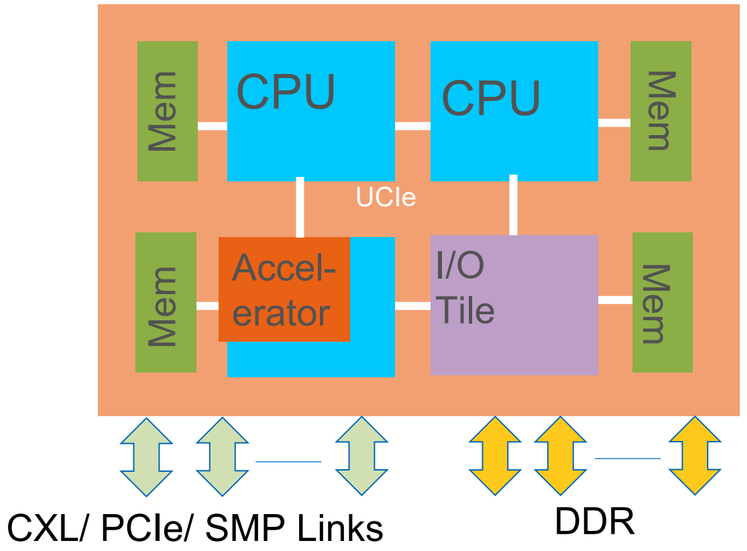
SoC as a Package level construct

- Standard and/ or Advanced package
- Homogeneous and/or heterogeneous chiplets
- Mix and match chiplets from multiple suppliers

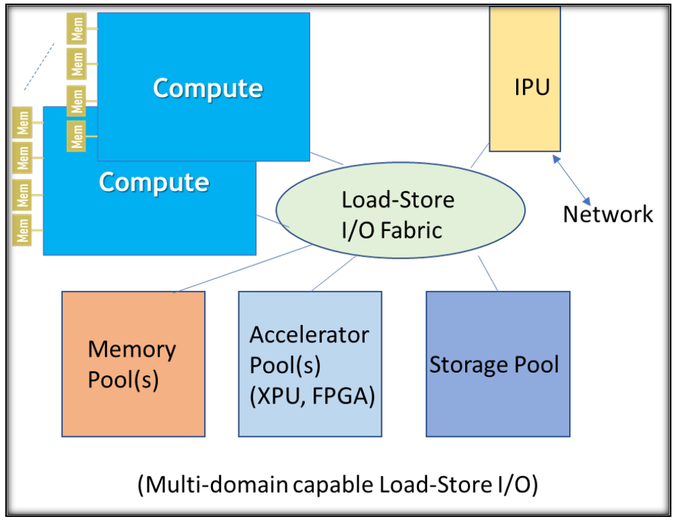
Across segments: Hand-held, Client, Server, Workstation, Comms, HPC, etc.

- Similar to PCIe/ CXL at board level



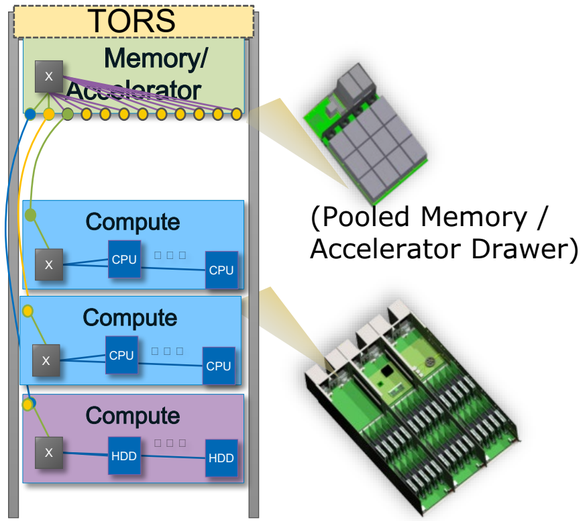


UCIe usage: Off-Package connectivity with UCIe Retimers



Vision: Load-Store I/O (CXL) as the fabric across the Pod providing low-latency and high bandwidth resource pooling/sharing as well as message passing.

(Pod of Racks)



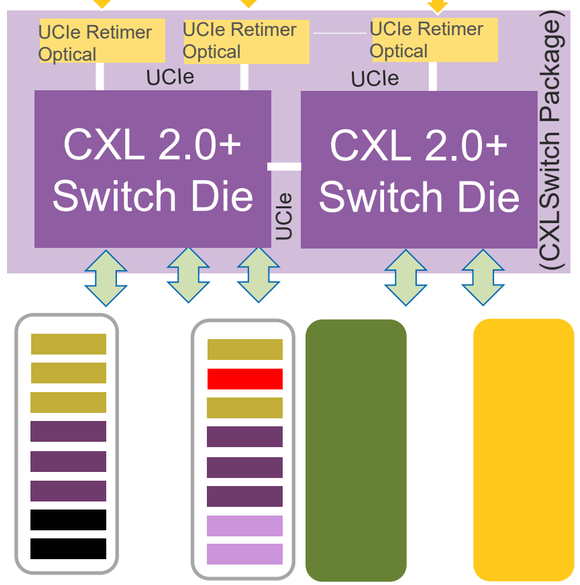
(Pooled Memory / Accelerator Drawer)

(Compute Drawer)

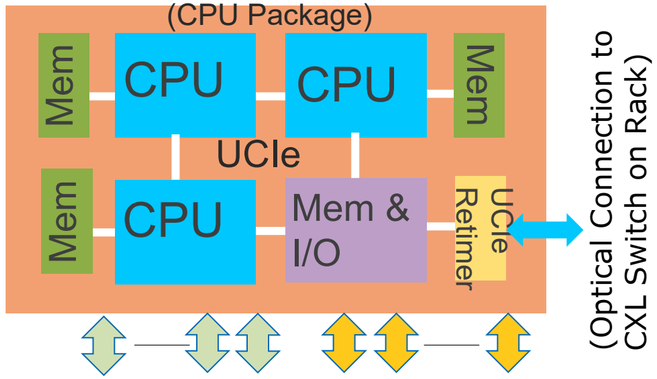
CXL Rack / Pod level connected using long-reach media (Electrical/ Optical/ ..) through UCIe Retimers (e.g., co-packaged optics)

(Physical Connectivity using UCIe-Retimer based co-packaged optics)

(Optical connections: Intra-Rack and Pod)



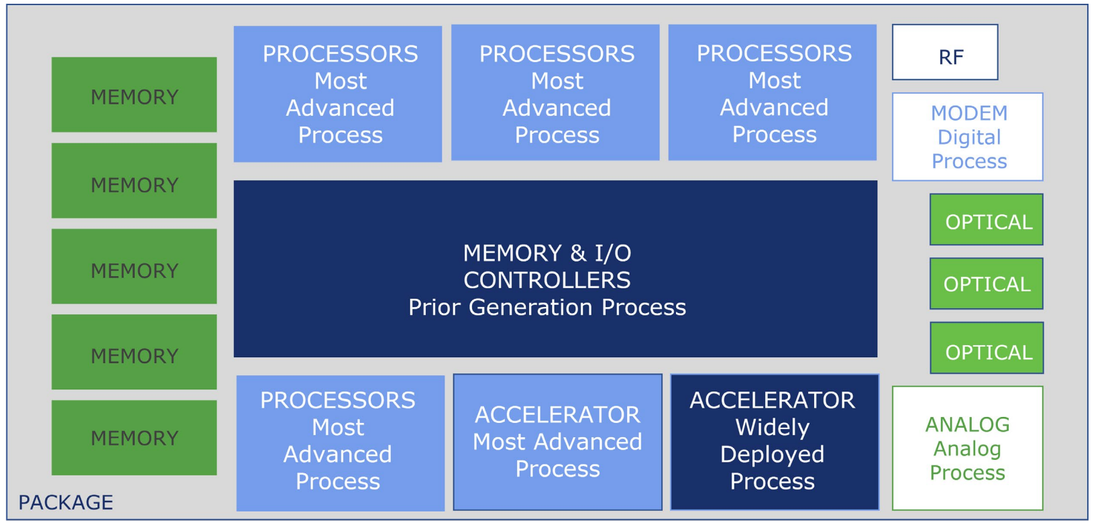
(Pooled/Shared Memory) (Pooled Accelerator)



(Interconnects at drawer level)

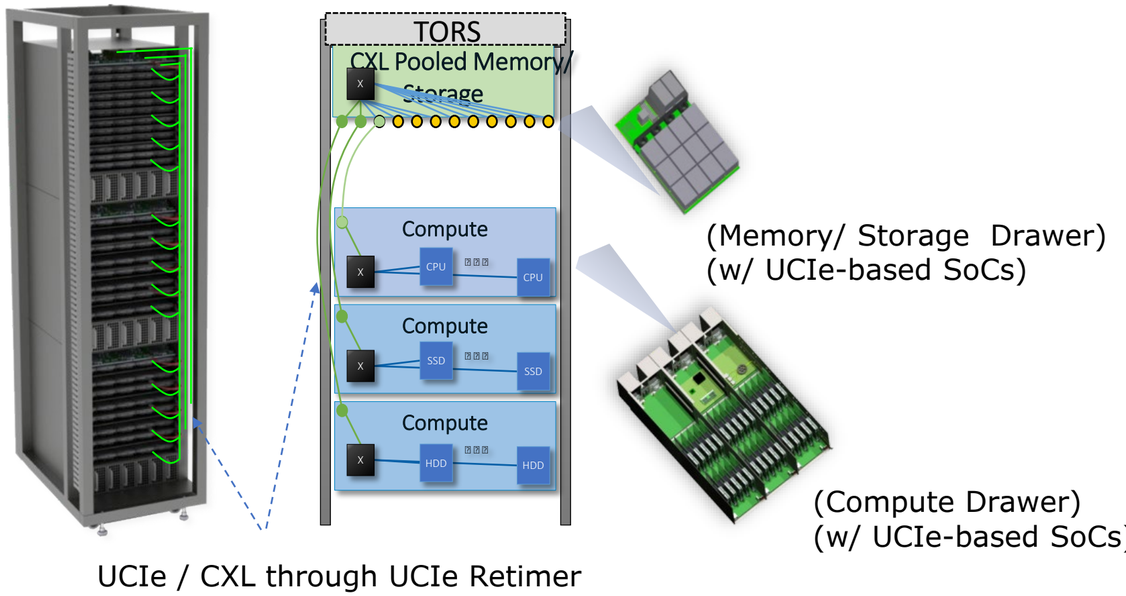
Rack/Pod Level resource pooling/ sharing with UCIe

Usage Models Supported by UCIe



SoC Package level construction for wide range of usages from Hand-held to high-end servers

✓ Mix and match dies from multiple sources with different packaging options



Provision to extend off-package with UCIe Retimers connecting to other media (e.g., optics, electrical cable, mmWave)

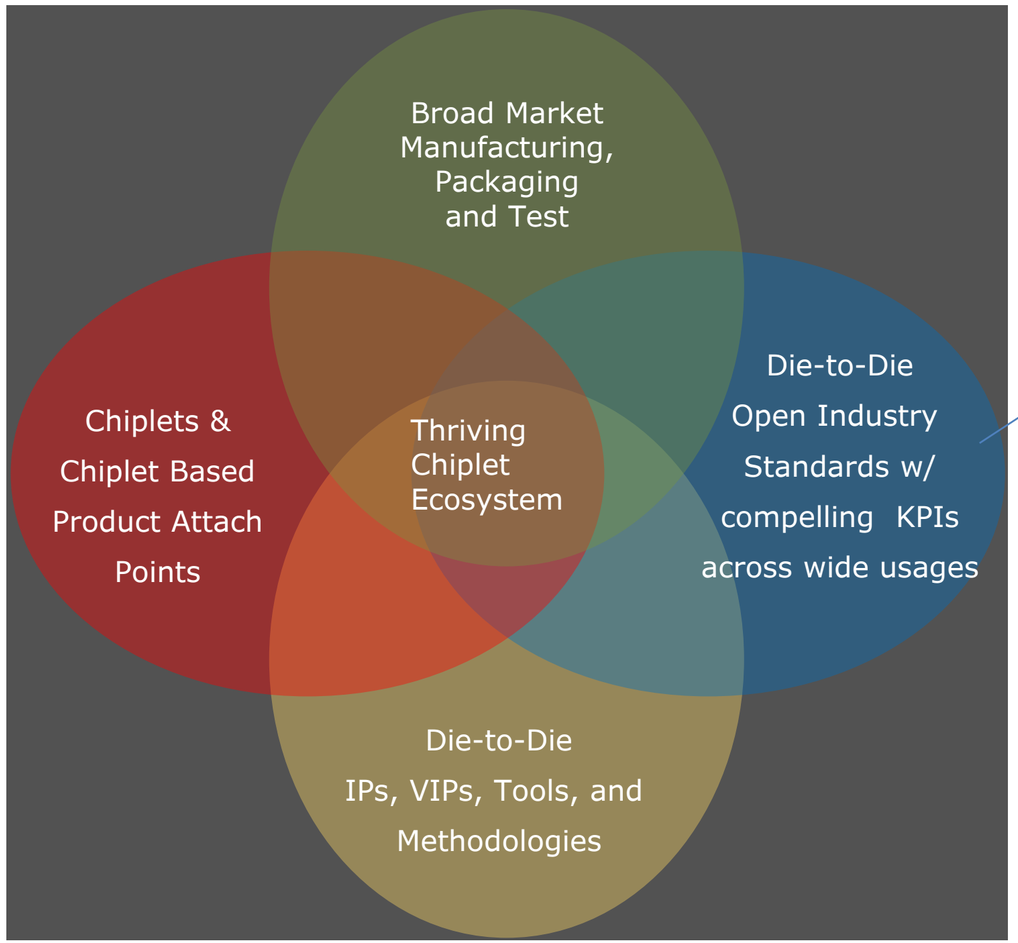
UCIe 1.0 delivers the best KPIs while meeting the projected needs for the next 5-6 years. Wide industry leader adoption spanning semiconductor, manufacturing, assembly, & cloud segments.

UCIe 1.0: Characteristics and Key Metrics

CHARACTERISTICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
Data Rate (GT/s)	4, 8, 12, 16, 24, 32		Lower speeds must be supported -interop (e.g., 4, 8, 12 for 12G device)
Width (each cluster)	16	64	Width degradation in Standard, spare lanes in Advanced
Bump Pitch (um)	100 – 130	25 - 55	Interoperate across bump pitches in each package type across nodes
Channel Reach (mm)	<= 25	<=2	

KPIs / TARGET FOR KEY METRICS	STANDARD PACKAGE	ADVANCED PACKAGE	COMMENTS
B/W Shoreline (GB/s/mm)	28 – 224	165 – 1317	Conservatively estimated: AP: 45u; Standard: 110u; Proportionate to data rate (4G – 32G)
B/W Density (GB/s/mm^2)	22-125	188-1350	
Power Efficiency target (pJ/b)	0.5	0.25	
Low-power entry/exit latency	0.5ns <=16G, 0.5-1ns >=24G		Power savings estimated at >= 85%
Latency (Tx + Rx)	< 2ns		Includes D2D Adapter and PHY (FDI to bump and back)
Reliability (FIT)	0 < FIT (Failure In Time) << 1		FIT: #failures in a billion hours (expecting ~1E-10) w/ UCIe Flit Mode

Ingredients of broad inter-operable chiplet ecosystem



D2D Specs

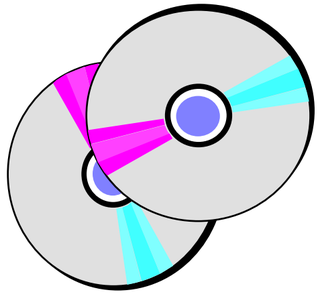
Well-defined Specs

(Electrical, Logical, Protocol (e.g., PCIe/ CXL)
Software, Form-Factor, Management)

C&I Test Spec

Test criteria based on Specs

(Test Definitions, Pass/Fail Criteria: Electrical, Logical, Protocol, Software)



Test Tools And Procedures

Test H/W & S/W
Validates
Test criteria
- Compliance
- Interoperability

PASS

FAIL

(Clear Test Output)

Predictable path to design compliance with UCIe

Organizational Update – July 2022

UCIe Consortium is now **incorporated!**

- Intellectual Property Rights (IPR) protection is in place for members.
  - Members include:
    - Adopters: Companies interested in building products
    - Contributors: Companies invested in helping to define future standards (working group participants)
    - Promoters: Board of Directors and leadership

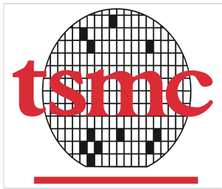
- New working groups have formed to support:
  - Electrical – exploring electrical solution elements (including mainband and sideband)
  - Protocol – advancing the protocol layer, D2D adapter, Logical PHY, and Interface
  - Form Factor/Compliance – furthering compliance, testing, and debugging, mechanical elements, Thermal, and forward-looking form-factor solutions (e.g., 3D)
  - Manageability/Security – exploring manageability extensions
  - Systems & Software – managing configuration and parameters
  - Marketing – outreach to the industry

We have welcomed two new Board members **Alibaba Group and NVIDIA!**

Board Members

Leaders in semiconductors, packaging, IP suppliers, foundries, and cloud service providers are joining together to drive
The open chiplet ecosystem.

JOIN US!



Agenda

- Interconnects in Compute Landscape
- UCIe (Universal Chiplet Interconnect Express): An Open Standard for Chiplets
- **Future Directions and Conclusions**

Summary

- **UCIe Consortium is now incorporated and introduced two newly-elected Board members Alibaba Group and NVIDIA.**

- **Chiplets and D2D interface are essential to the compute continuum**
  - Power-efficient performance, yield optimization, different functions, custom solutions, cost-effective

- **UCIe standardization will propel the development an open ecosystem**
  - Open plug-and-play “slot” at package level will unleash innovations
  - Evolution needs to track the underlying packaging technology to deliver compelling metrics

- **Form-factor, New Protocols, and manageability are some other areas for innovation**
- UCIe Consortium welcomes interested companies and institutions to join the organization at the **Contributor** and **Adopter level**.

- Established **5 Technical Working Groups** (Electrical, Protocol, Form Factor/Compliance, Manageability / Security, Systems and Software) and **Marketing Working Group**

- **Learn more by visiting** www.UCIexpress.org

Thank You

www.UCIexpress.org